

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.                      Art Unit: 2181  
Serial No.: 10/069,195                                      Examiner: Vincent Lai  
Filed : November 7, 2002  
Assignee : Intel Corporation  
Title : BRANCH INSTRUCTION FOR PROCESSOR

**MAIL STOP RCE**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made with a Request for Continued Examination (RCE). No fee is required.

Enclosed documents listed on the herewith Form PTO-1449 were cited in the attached European Search Report dated July 20, 2006, issued in a foreign counterpart application. To the best knowledge of the undersigned, this is the first citation of these items in any communication from a foreign patent office in a counterpart foreign application.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the

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Attorney's Docket No. 10559-304US1  
P9625US

Examiner's initials in the left column per MPEP 609 are  
earnestly solicited along with an early action on the merits.

Please apply any credits or additional charges to deposit  
account 06-1050.

Respectfully submitted,

Date: February 26, 2007

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-304US1	Application No. 10/069,195
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date November 7, 2002	Group Art Unit 2181

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0038403	03/2002	Wolrich et al.			
	AB	3,881,173	04/1975	Larsen et al.			
	AC	4,454,595	06/1984	Cage			
	AD	4,477,872	10/1984	Losq et al.			
	AE	4,569,016	02/1986	Hao et al.			
	AF	4,742,451	05/1988	Bruckert et al.			
	AG	4,755,966	07/1988	Lee et al.			
	AH	4,808,988	02/1989	Burke et al.			
	AI	4,816,913	03/1989	Harney et al.			
	AJ	4,847,755	07/1989	Morrison et al.			
	AK	4,868,735	09/1989	Moller et al.			
	AL	4,992,934	02/1991	Portanova et al.			
	AM	5,045,995	09/1991	Levinthal et al.			
	AN	5,056,015	10/1991	Baldwin et al.			
	AO	5,165,025	11/1992	Lass			
	AP	5,170,484	12/1992	Grondalski			
	AQ	5,187,800	02/1993	Sutherland			
	AR	5,189,636	02/1993	Patti et al.			
	AS	5,202,972	04/1993	Gusefski et al.			
	AT	5,220,669	06/1993	Baum et al.			
	AU	5,247,671	09/1993	Adkins et al.			
	AV	5,274,770	12/1993	Khim Yeoh et al.			
	AW	5,394,530	02/1995	Kitta			
	AX	5,428,779	06/1995	Allegrucci et al.			
	AY	5,450,603	09/1995	Davies			
	AZ	5,463,746	10/1995	Brodnax et al.			
	BA	5,509,130	04/1996	Trauben et al.			

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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	BB	5,541,920	07/1996	Angle et al.			
	BC	5,544,337	08/1996	Beard et al.			
	BD	5,572,690	11/1996	Molnar et al.			
	BE	5,600,848	02/1997	Sproull et al.			
	BF	5,610,864	03/1997	Manning			
	BG	5,640,538	06/1997	Dyer et al.			
	BH	5,669,012	09/1997	Shimizu et al.			
	BI	5,680,564	10/1997	Divivier et al.			
	BJ	5,701,435	12/1997	Chi			
	BK	5,724,563	03/1998	Hasegawa			
	BL	5,748,950	05/1998	White et al.			
	BM	5,802,373	09/1998	Yates et al.			
	BN	5,812,811	09/1998	Dubey et al.			
	BO	5,815,698	09/1998	Holmann et al.			
	BP	5,815,714	09/1998	Shridhar et al.			
	BQ	5,819,080	10/1998	Dutton et al.			
	BR	5,832,258	11/1998	Kiuchi et al.			
	BS	5,838,975	11/1998	Abramson et al.			
	BT	5,848,276	12/1998	King et al.			
	BU	5,857,104	01/1999	Natarjan et al.			
	BV	5,870,597	02/1999	Panwar et al.			
	BW	5,872,963	02/1999	Bitar et al.			
	BX	5,875,470	02/1999	Dreibelbis et al.			
	BY	5,898,866	04/1999	Atkins et al.			
	BZ	5,900,025	05/1999	Sollars			
	CA	5,923,872	07/1999	Chrysos et al.			
	CB	5,926,646	07/1999	Pickett et al.			

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	CC	5,928,358	07/1999	Takayama et al.			
	CD	5,937,177	08/1999	Molnar et al.			
	CE	5,943,491	08/1999	Sutherland et al.			
	CF	5,944,816	08/1999	Dutton et al.			
	CG	5,946,222	08/1999	Redford			
	CH	5,956,514	09/1999	Wen et al.			
	CI	5,993,627	11/1999	Anderson et al.			
	CJ	6,005,575	12/1999	Colleran et al.			
	CK	6,009,505	12/1999	Thayer et al.			
	CL	6,061,710	05/2000	Eickemeyer et al.			
	CM	6,061,711	05/2000	Song et al.			
	CN	6,101,599	08/2000	Wright et al.			
	CO	6,115,777	09/2000	Zahir et al.			
	CP	6,139,199	10/2000	Rodriguez			
	CQ	6,141,348	10/2000	Muntz			
	CR	6,145,123	11/2000	Torrey et al.			
	CS	6,157,988	12/2000	Dowling			
	CT	6,195,739	02/2001	Wright et al.			
	CU	6,205,468	03/2001	Diepstraten et al.			
	CV	6,223,208	04/2001	Kiefer et al.			
	CW	6,223,277	04/2001	Karguth			
	CX	6,230,119	05/2001	Mitchell			
	CY	6,230,230	05/2001	Joy et al.			
	CZ	6,230,261	05/2001	Henry et al.			
	DA	6,259,699	07/2001	Opalka et al.			
	DB	6,269,391	07/2001	Gillespie			
	DC	6,275,508	08/2001	Aggarwal et al.			

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	DD	6,279,066	08/2001	Velinger			
	DE	6,314,510	11/2001	Saulsbury et al.			
	DF	6,338,133	01/2002	Schroter			
	DG	6,378,124	04/2002	Bates et al.			
	DH	6,378,125	04/2002	Bates et al.			
	DI	6,401,155	06/2002	Saville et al.			
	DJ	6,408,325	06/2002	Shaylor			
	DK	6,446,190	09/2002	Barry et al.			
	DL	6,496,847	12/2002	Bugnion et al.			
	DM	6,505,229	01/2003	Turner et al.			
	DN	6,523,108	02/2003	James et al.			
	DO	6,543,049	04/2003	Bates et al.			
	DP	6,560,629	05/2003	Harris			
	DQ	6,560,671	05/2003	Samra et al.			
	DR	6,564,316	05/2003	Perets et al.			
	DS	6,574,702	06/2003	Khanna et al.			
	DT	6,697,935	02/2004	Borkenhagen et al.			
	DU	6,862,676	03/2005	Knapp et al.			
	DV	6,976,095	12/2005	Wolrich et al.			
	DW	6,983,350	01/2006	Adiletta et al.			
	DX	7,020,871	03/2006	Bernstein et al.			

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	DY	0 130 381	01/1985	Europe				
	DZ	0 463 855	01/1992	Europe				
	EA	0 476 628	03/1992	Europe				

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### Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	EB	0 696 772	02/1996	Europe				
	EC	59-111533	06/1984	Japan (abstract only)				X
	ED	WO03/019399	03/2003	WIPO				
	EE	WO03/085517	10/2003	WIPO				

### Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	EF	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
	EG	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: <a href="http://www.romilly.co.uk/whathart.htm">http://www.romilly.co.uk/whathart.htm</a> >
	EH	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", <i>IEEE</i> , pp. 57-62, (1996).
	EI	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
	EJ	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
	EK	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
	EL	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
	EM	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM &amp; IEEE-CS</i> , 20(2):136-145, May 1992.
	EN	Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
	EO	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).
	EP	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , <i>IEEE</i> , pp. 26-31 (1996).
	EQ	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	ER	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	ES	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
	ET	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).

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**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	EU	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
	EV	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27<sup>th</sup> Annual Hawaiian International Conference on System Sciences, IEEE</i> , pp. 584-593, (1994).
	EW	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	EX	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
	EY	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
	EZ	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
	FA	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

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